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Sol–Gel Solution-Deposited InGaZnO Thin Film Transistors

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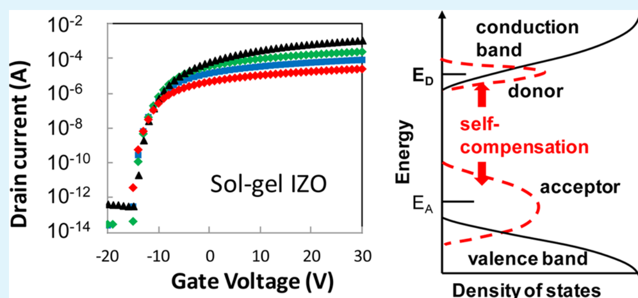
ABSTRACT: Thin film transistors (TFTs) fabricated by solution processing of sol–gel oxide semiconductor precursors in the group In–Ga–Zn are described. The TFT mobility varies over a wide range depending on the precursor materials, the composition, and the processing variables, with the highest mobility being about 30 $cm^2/(V\ s)$ for IZO and 20 $cm^2/(V\ s)$ for IGZO. The positive dark bias stress effect decreases markedly as the mobility increases and the high mobility devices are quite stable. The negative bias illumination stress effect is also weaker in the higher mobility TFTs, and some different characteristic properties are observed. The TFT mobility, threshold voltage, and bias stress properties are discussed in terms of the formation of self-compensated donor and acceptor states, based on the chemistry and thermodynamics of the sol–gel process.



KEYWORDS: *sol–gel oxides, IGZO, thin film transistors, self-compensation, bias stress*

1. INTRODUCTION

Metal oxide semiconductor devices are developing rapidly, with the primary application for thin film transistor (TFT) display backplanes. The attraction of the oxides is the high mobility that enables their use for OLED displays or high speed LCD switching. Since the first report in 2004,[1] it is notable that high mobility is observed in amorphous oxide alloys such as InGaZnO (IGZO)[2,3] as well as polycrystalline oxides.[4,5] The origin of the high mobility is the metal s-orbitals that are relatively insensitive to bond angle disorder compared to a covalent semiconductor such as amorphous silicon. The amorphous oxides have very few localized band tail states and hence are dominated by band conduction rather than multiple trapping.

Solution deposition methods are attractive for low cost manufacturing of large area electronics, and so there is interest in the formation of the oxide semiconductors from solution. The main approach has been to use a sol–gel process with various precursor chemicals,[4,6−11] and this is the method used for the devices described in this paper. The coated films generally must be annealed at a relatively high temperature of 300−500 °C to densify the film, which is a suitable temperature range for glass substrates but not for most plastics. Alternative solution precursors have been developed for low temperature processing, based on either exothermic reactions of the materials during annealing,[12] photochemical activation,[13] or approaches that enhance hydrolysis reaction.[14−16] Several papers report TFT data for solution oxides with mobility and other properties that vary widely. The work described here compares two alternative chemical precursor types and a range of compositions in the InGaZn group of metals. We also compare results from alternative TFT processing techniques, with various gate dielectrics, source-drain metals, TFT geometry, and patterning approaches. Gate bias stress effects with and without illumination are also reported.

There has been much discussion about the presence and role of deep defect or impurity states in the oxides. A characteristic feature of these materials is that they can be heavily n-type conductors or nearly intrinsic semiconductors. It was widely assumed that the source of the n-type doping was oxygen vacancies,[17,18] for which control of the oxygen stoichiometry was the key to forming semiconducting materials. Control of the oxygen atmosphere for sputtered metal oxides is indeed essential to form semiconducting films. However, theoretical calculations show that the oxygen vacancy is a deep donor and so is not able to account for the highly conducting n-type materials. Instead calculations show that hydrogen is a shallow donor and this was proposed to be the origin of the n-type doping in ZnO[19−21] and other oxides.[22,23] Hydrogen is easily introduced from the residual gas in a deposition system or from device annealing which is often done in humid air. Many oxides cannot be doped p-type and a common explanation is self-compensation by native defects, since the formation energy of a charged defect depends on the position of the Fermi energy.[24] This mechanism is used to explain the present results as discussed below.

Received: January 9, 2014
Accepted: March 4, 2014
Published: March 4, 2014

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The oxide semiconductors have a particular property of a significant gate bias stress response with the combination of negative gate bias and white light illumination (NBIS).[25,26] The origin of the NBIS, which is a form of persistent photoconductivity, apparently results from the optical excitation of electrons from deep states into the TFT channel, and the formation of a barrier to their recapture. One of the models for NBIS involves the deep oxygen vacancy, which is postulated to have a negative correlation energy giving it a large barrier for recapture of the electron. There are, however, other models, including hole trapping in the gate dielectric.[27] Recent work suggests that the oxygen interstitial might be the relevant state for the NBIS effect. The interstitial is a deep acceptor with electronic transitions in the lower half of the band gap.[28]

These defects are particularly relevant to the solution oxide materials. Most of the precursor materials are metal nitrate hydrates, of the form $M(NO_3)_x \cdot nH_2O$. The thermal annealing process to form the final compound is therefore a process of eliminating oxygen, nitrogen, and hydrogen as the material densifies toward the target oxide composition. Hence, it is highly likely that any or all of hydrogen, oxygen vacancies, and oxygen interstitials will be present as well as possible nitrogen defects and other deep states. The trends that are observed in the solution oxides might give information about the role of the alternative defects in both these materials and in the sputtered films.

2. EXPERIMENTAL METHODS

2.1. Fabrication Methods. The materials studied are in the InGaZn group, and Figure 1a illustrates the range of compositions.

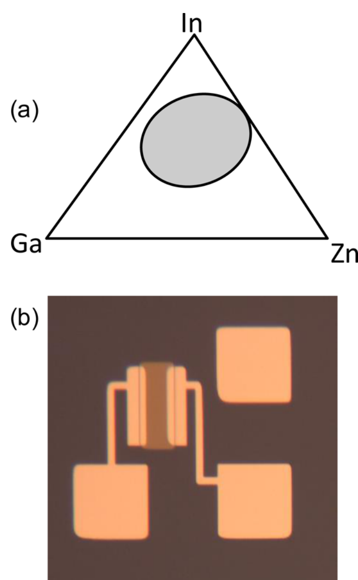

Figure 1. (a) Illustration of the ternary In−Ga−Zn system, indicating the composition range of samples used in this study. (b) Optical micrograph of a typical TFT on Si/SiO_2, made with the etch stop process.

Most of the measurements are for a small set of specific compositions which gave the best TFT performance, with fewer measurements at other compositions for comparison. The composition dependence of the TFT properties will be described in a future paper in much more detail and also covers a wider materials set.

The oxide precursor solutions were mostly prepared from metal nitrates purchased from Aldrich and selected because of their low decomposition temperatures.[29] In the case of zinc, we explored the acetate and the nitrate precursor, and compared their performance. The solution compositions are shown in Table 1, and all of the solutions were at 0.1 M concentration in anhydrous 2-methoxyethanol solvent. The precursor solutions were stirred for 1 h at 80 °C before use. Each solution was spin-coated to form films ranging from 7 to 20 nm in thickness. The films were heated in air at 110 °C for 5 min, and subsequently annealed in the range 350−500 °C for 1 h in ambient air. While the humidity was not carefully controlled, the best results seem to correspond to an ambient humidity of about 50%. In some cases, thicker oxide films were prepared by using two or three spin-coats with the high temperature anneal in between each deposition.

The high temperature anneal densifies the film and thermogravimetric analysis showed that weight loss was complete at 300−350 °C. X-ray photoemission analysis showed that the metal composition of the annealed film is similar to the composition of the solution. X-ray diffraction and atomic force microscopy indicate that the films are amorphous.

2.2. Materials and Device Processing and Measurement. The transistors were all top-contact, bottom-gate structures. Initial evaluation and selection of the material was performed with films spin-coated on silicon oxide followed by source-drain contacts evaporated through a shadow mask. The focus of the project was then to explore how the device processing influenced the TFT performance and to develop a process flow suitable for backplane fabrication. The gate dielectric was usually either 100 nm of thermally grown silicon dioxide on a silicon wafer (Si/SiO_2), or a stack of silicon dioxide and silicon nitride deposited by plasma-enhanced chemical vapor deposition (PECVD) on a glass substrate. A few measurements with Al_2O_3 and Ta_2O_5 gate dielectric deposited by atomic layer deposition were made for further comparison. The semiconductor films were patterned by dry reactive-ion etching. The source and drain electrodes were sputtered metals patterned by wet etching or lift-off process. After the structure is completed, the transistors were annealed in air at 180 °C for 30 min. Various patterning techniques were investigated, including lift-off of the S/D metal, a back-channel etch (BCE) process, or an etch stop (ES) process. Figure 1b is a micrograph of a typical etch stop device on Si/SiO_2. For lift-off or BCE, some devices were left with no passivation and some had a deposited organic material as a passivation layer. Some samples were hydrogenated by atomic hydrogen in a plasma system, but the process degraded the devices, possibly due to ultraviolet damage from the plasma rather than the intrinsic effect of hydrogen.

The TFTs were tested using a standard probe system, and measurements were primarily taken of the transfer characteristics with a range of drain voltages covering the linear and saturation regimes. Most measurements were quasi-static, but pulsed gate and drain voltages were used for particularly unstable devices. The mobility was calculated by applying the conventional TFT models based on the gradual channel approximation. Gate bias stress was measured for periods of up to 5 h at various gate and drain voltages. The illumination stress (NBIS) was performed with a white light microscope illuminator.

3. TFT MEASUREMENT RESULTS

Our investigation found that devices fabricated with the Zn nitrate precursor gave substantially better TFT performance compared to devices made with the acetate precursor, with mobility 5−10 times higher. Preliminary studies[13] indicated that the optimum composition for IGZO was the ratio 70:15:15 In:Ga:Zn (by molar concentration, see Table 1) and 60:40 In:Zn for IZO, and hence, most of the measurements were made using these compositions. Figure 2 shows examples of IGZO TFT characteristics for a device fabricated on Si/SiO_2 and annealed at 400 °C. After the oxide semiconductor island was patterned, the etch stop process was used in which a PECVD oxide cap was deposited and patterned and then the Ti(300 Å)/Au(800 Å) source-drain contacts were deposited, which were patterned by etching. The mobility is in the range

Table 1. Composition of Oxide Precursor Solutions in Molar Concentration[a]

channel material	indium nitrate hydrate	gallium nitrate hydrate	zinc acetate dihydrate	zinc nitrate hexahydrate
IGZO (68:10:22)	0.085 M (511.4 mg)	0.125 M (63.9 mg)	0.0275 M (120.7 mg)	
IGZO (60:10:30)	0.075 M (338.4 mg)	0.0125 M (48.0 mg)	0.0375 M (123.5 mg)	
IGZO (75:5:20)	0.09375 M (564.1 mg)	0.0625 M (32.0 mg)	0.025 M (109.8 mg)	
IGZO (70:15:15)	0.070 M (315.87 mg)	0.015 M (57.54 mg)		0.015 M (66.94 mg)
IGZO (60:20:20)	0.060 M (270.75 mg)	0.020 M (76.72 mg)		0.020 M (89.25 mg)
IGZO (34:33:33)	0.034 M (153.42 mg)	0.033 M (126.59 mg)		0.033 M (147.26 mg)
IZO (60:40)	0.060 M (270.75 mg)			0.040 M (178.49 mg)

[a]Numbers in parentheses indicate the weight amount used per 15 mL of 2-methoxyethanol solvent.

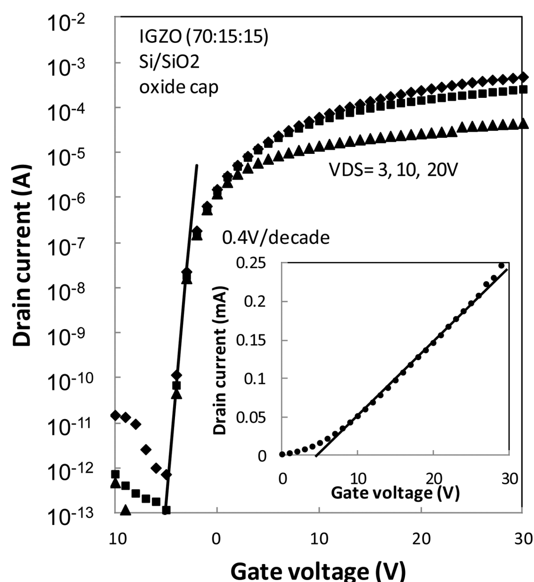

Figure 2. TFT transfer characteristics at the indicated drain voltages for 70:15:15 IGZO composition with the Zn nitrate precursor using the sol−gel process. The TFT is fabricated on a Si/SiO_2 dielectric with the etch stop process. The inset shows the 10 V characteristic on a linear scale.

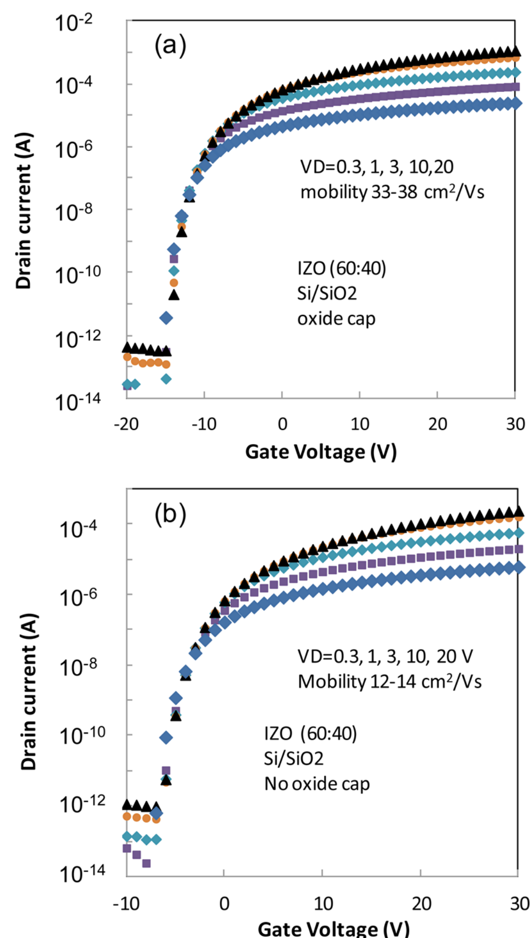

Figure 3. TFT characteristics of 60:40 IZO composition made with Zn nitrate precursor. (a) TFT fabricated on Si/SiO_2 with an oxide cap. (b) Same device process without the oxide cap.

10−20 $cm^2/(V\ s)$, the turn-on voltage is about −5 V, the threshold voltage is close to 0 V, and the subthreshold slope is 0.4 V/decade. The leakage current is in the pA range or less. The mobility showed some variation with source-drain voltage presumably because of contact resistance and also depends on the oxide thickness and the general variability of the process.

IZO devices shown in Figures 3 and 4 were also made with the nitrate precursor and gave an even higher mobility of 20−40 $cm^2/(V\ s)$. The device in Figure 3a was fabricated on Si/SiO_2 using the same etch stop process as for the IGZO devices in Figure 2. The device in Figure 3b does not have the oxide cap and uses the lift-off process to pattern the source-drain contacts. This comparison shows that the oxide cap substantially increases the mobility which we associate with it providing protection from later processing and from the ambient. The data in Figure 4 is for an IZO device fabricated on glass with gate contact patterned by photolithography and PECVD nitride/oxide gate dielectric, and using the same etch stop process as for Figure 3a. The mobility is slightly less that the devices on Si/SiO_2, but otherwise the transfer characteristics are similar. Figure 4b shows the turn-on region in greater detail with a subthreshold slope of 0.24 V/decade.

Figure 5a shows TFT transfer characteristics of one of the better IGZO devices using the Zn acetate precursor and fabricated on Si/SiO_2 which was annealed at 350 °C. The TFT mobility is 3 $cm^2/(V\ s)$ with a turn-on voltage of −3 V. The subthreshold slope of about 0.3 V/decade is similar to the higher mobility devices with the nitrate precursor and suggests that the presence of shallow localized states is not the cause of the reduced mobility. Figure 5b shows the characteristics of an acetate precursor IGZO TFT fabricated on glass with lithographically patterned gate metal, a Ta_2O_5/PECVD Si oxide gate dielectric, and source-drain contacts patterned by lift-off. The mobility is about 1 $cm^2/(V\ s)$, with a larger subthreshold slope and leakage current but otherwise similar properties. The acetate precursor devices were made before the nitrate precursor devices and before the oxide cap etch stop process was developed, which may be a partial explanation of the lower mobility. Similar IZO TFTs using the acetate precursor also had low mobility no greater than 2 $cm^2/(V\ s)$.

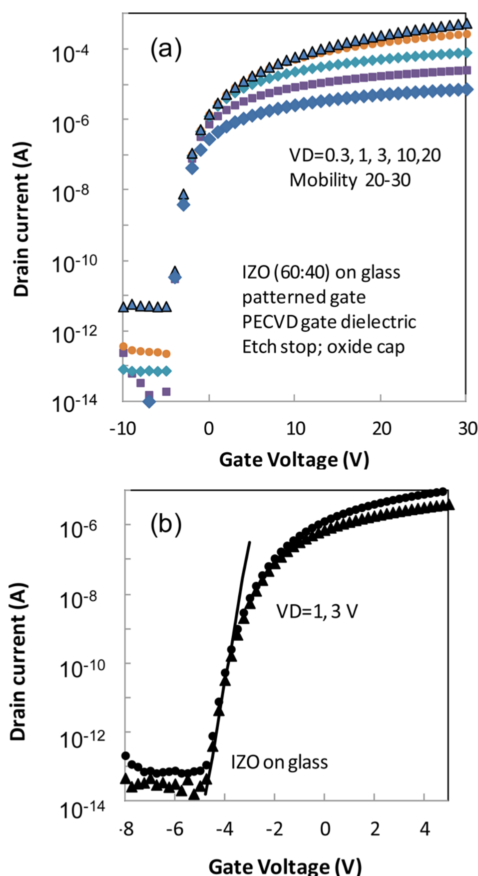

Figure 4. TFT characteristics of 60:40 IZO composition made with Zn nitrate precursor. (a) TFT fabricated on glass with PECVD silicon nitride/oxide gate dielectric and an etch stop process with an oxide cap. (b) Characteristics measured over a smaller gate voltage range to show the turn-on region more clearly.

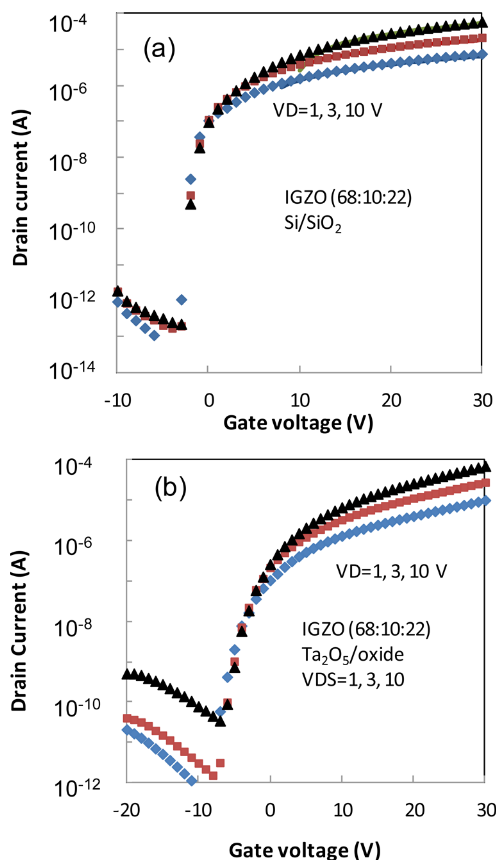

Figure 5. TFT characteristics of 68:10:22 IGZO composition with Zn acetate precursor in the sol−gel process. (a) TFT fabricated on Si/SiO_2 gate dielectric. (b) TFT fabricated on glass with Ta_2O_5/oxide gate dielectric.

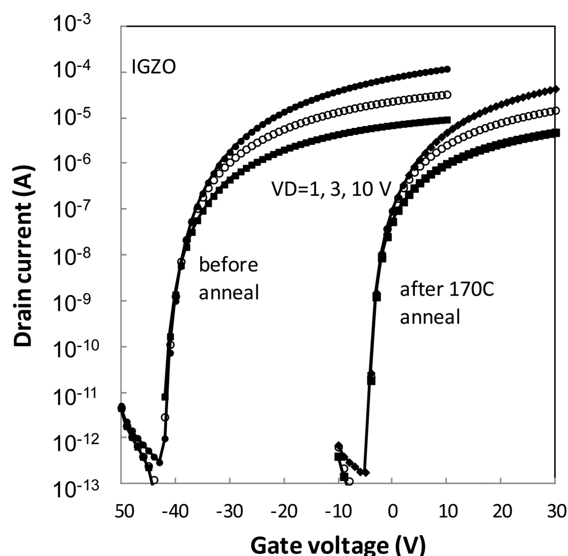

Figure 6. TFT characteristics of 68:10:22 IGZO comparison before (lines) and after (points) annealing at 170 °C for 30 min.

The TFT properties varied substantially between the various devices, depending on the oxide semiconductor composition, and the details of the process that was used. Source-drain contacts, the thickness of the oxide, the patterning technique, the passivation and the annealing temperature were all factors that affected the TFT characteristics to some degree. The patterning of the source-drain contacts was found to be particularly important, with the BCE process generally resulting in lower mobility than the lift-off or etch stop process, presumably due to damage of the channel by the etch. The shadow mask deposition of the contacts used in the initial evaluation gave high mobility, comparable to the etch stop process.

The TFT turn-on voltage of all the devices also varied over a range of voltages: the examples in Figures 2 and 3 have turn-on voltages from −4 to −15 V, but in other devices we have observed values as high as −40 V. The turn-on voltage was controlled by a combination of the dielectric material and thicknesses and in particular by the low temperature anneal. In general, the Si/SiO_2 gate dielectric gave a more negative V_{ON} than the PECVD nitride/oxide gate dielectric, but other processing and exposure factors made a difference too. The final anneal at 150−200 °C was needed to move V_{ON} toward 0 V, and the possible mechanism is discussed below. Figure 6 shows an example of an IGZO TFT fabricated with the nitrate precursor, before and after a 170 °C anneal for 30 min which causes V_{ON} to change by about 40 V. Similar results were found for IZO.

Two spin-coats of the oxide semiconductor generally improved the mobility slightly, giving a thickness of 30−40 nm, but further increase of oxide thickness showed no further gains in performance. Compositional studies indicated that the

dx.doi.org/10.1021/am500126b | ACS Appl. Mater. Interfaces 2014, 6, 4428−4437

optimum IGZO composition was 70:15:15 for the nitrate precursor and 68:10:22 for the acetate precursor. Various compositions were studied around the 68:10:22 IGZO material, but we found that 60:10:30 and 75:5:20 compositions both gave substantially lower TFT mobility, as did 34:33:33 and 25:50:25 compositions. These last two values correspond to compositions commonly used for sputtered IGZO. Hence, both the 70:15:15 and 68:10:22 compositions are substantially different from the optimum TFT performance of sputtered IGZO.

3.1. Gate Bias Stress Measurements. The gate bias stress characteristics were studied in a wide range of TFTs, focusing primarily on positive voltage stress in the dark and negative bias stress under illumination. Examples of the positive dark bias stress are shown in Figure 7 for samples covering a wide range of mobility and for the two Zn precursor systems and both IGZO and IZO. The gate bias voltage was 30 V, and source-drain voltage 3 or 5 V. There is an evident correlation between the mobility and the rate of bias stress, with very low mobility devices being highly unstable and high mobility devices being very stable. There is no obvious correlation with the gate dielectric as both Si/SiO_2 and PECVD nitride/oxide dielectrics showed both high and low stress according to the mobility of the TFT. The stress effects were recovered by annealing at 150−200 °C for about 1−3 h and more slowly at room temperature.

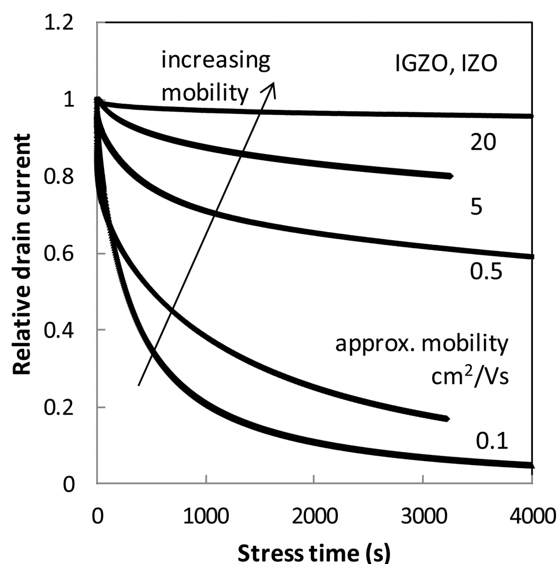

Figure 7. Examples of the positive gate voltage bias stress time dependence for the sol−gel IGZO and IZO oxides TFTs with a range of mobility values.

NBIS measurements were performed in air at room temperature using a white light microscope Illuminator and a gate bias of typically −30 V. The magnitude of the effect and its characteristic behavior varied greatly for the different devices. The higher mobility devices made with the Zn nitrate precursor show the generally expected behavior as indicated in Figure 8a for IGZO and Figure 8b for IZO. The NBIS in the IGZO device exhibited an increasing negative V_{ON} as the illumination time increased. Annealing at 150−200 °C reduced V_{ON} until it eventually recovered the original state. The NBIS in high mobility IZO showed a much smaller negative shift of only 3−5 V for the same illumination time. With longer illumination, the shift in the turn-on voltage changed direction and becomes positive. Annealing at 150−200 °C again restores the initial state.

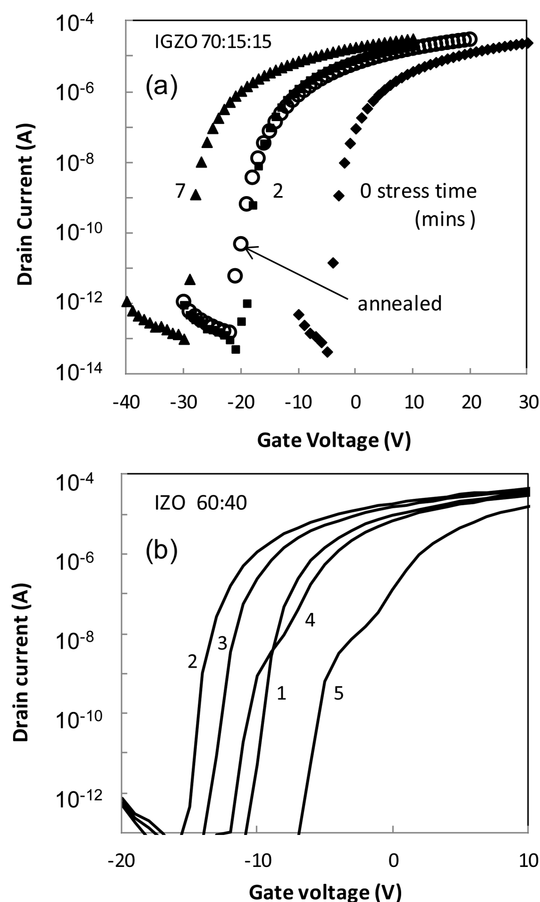

Figure 8. (a) NBIS data and the effect of annealing for nitrate precursor IGZO with high mobility. (b) NBIS data and the effect of annealing for nitrate precursor IZO with high mobility.

The lower mobility TFTs including IGZO made with the Zn acetate precursor had more surprising and unusual NBIS properties. This was observed for both IGZO and IZO, and is shown in Figure 9 for an IGZO TFT with mobility ~1 $cm^2/(V\ s)$. The initial measurement was for a device on Si/SiO_2 which was annealed to 180 °C and had a V_{ON} of close to 0 V (data set 1 in Figure 9). The device was subjected to NBIS with V_G = −30 V, with the source and drain contacts connected but with zero source-drain bias voltage, and white light intensity of ~100 mW/cm^2 for 2 min, after which V_{ON} was about −20 V (data set 2). An adjacent device was subject to the same gate voltage and illumination but with unconnected source-drain contacts, and after the stress this TFT showed only a small change in V_{ON} (data set A). The TFTs were then annealed at 240 °C for 6 min and remeasured. After the anneal, V_{ON} was even more negative at about −40 to 50 V, (data set 3), and we find that the uncontacted TFT had also shifted to a similar large negative V_{ON} (data set B). Further annealing at 240 °C for 10 min (data set 4) and 2 h (data set 5) reduced V_{ON}, and eventually it recovered to its initial value, and the same cycle could be repeated. We also confirmed that annealing alone does not give any negative shift, but that illumination at zero gate bias can give a negative shift.

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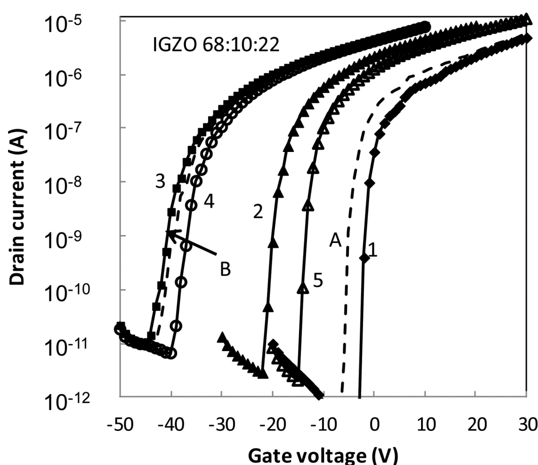


Figure 9. Examples of the negative bias illumination stress (NBIS) and the effects of annealing for a low mobility IGZO TFT made with the Zn acetate precursor. Data sets 1−5 are for a TFT contacted during NBIS, and data sets A and B are for a adjacent TFT without contacted source and drain.

4. DISCUSSION

The data for the sol−gel IGZO and IZO TFTs in Figures 2−4 compare well with devices fabricated by sputtering which have mobility values in the same general range. We show that the etch stop process results in TFTs that have sharp turn-on characteristics, low threshold voltage, and stable performance. The solution oxides therefore offer TFT performance characteristics that meets the mobility required for an OLED backplane.

There is some indication that the higher mobility TFTs may have larger negative turn-on voltages, although the variation is large and the low temperature thermal annealing to reduce the turn-on voltage was not optimized. A negative turn-on voltage allows for a depletion mode device and could give an increased mobility because the current flow is further from the interface. However TFT applications usually require accumulation mode devices.

4.1. Interpretation of Material Dependence of TFT Properties. The main observation with regard to the TFT characteristics is that the mobility varies by a factor 100 or more depending on the material and the processing conditions, and the onset voltage also varies widely. There are several different possible explanations of the differing mobility. For example, a more disordered semiconductor material may have a wider band tail which traps carriers and hence reduces the mobility. A broader band tail will typically give a larger subthreshold slope because the shift in Fermi energy as the gate voltage changes is limited by the presence of localized states. However, while the subthreshold slope varies in the different samples, there is no obvious correlation with the mobility. For example, the device of Figure 5a has a considerably lower mobility than the device of Figure 2, but both have similarly small subthreshold slope. Hence, band tail disorder is apparently not the main origin of the different mobility. An alternative mechanism is a possible effect of the dielectric interface, in which a rough interface can reduce the mobility by enhanced scattering. However, the same Si/SiO_2 dielectric gives both high and low mobility and hence is also not the origin of the variable mobility.

The mobility of the oxides has been analyzed in terms of a percolation model,[30] based on fluctuations in the local fixed charge distribution, possibly arising from the atomic disorder within the ionic oxide material. The potential fluctuations restrict the possible conduction paths and hence limit the mobility. For different materials and processing conditions, it is reasonable to suppose that there are different degrees of charge disorder and hence the percolation model is a reasonable explanation of the varying mobility.

The variation in the turn-on voltage is also related to fixed charges in the device. Experiments shows that some control of the fixed charge is evidently associated with the choice of the dielectric, but we also see a large variation in V_{ON} with a single type of dielectric (i.e., either Si/SiO_2 or PECVD nitride/oxide). Furthermore, V_{ON} is adjusted by the final anneal at 150−200 °C and for most devices can be brought to the range between zero and −10 V. A large negative V_{ON} implies the presence of shallow dopant states in the oxide since a large shift in V_{ON} is unlikely to originate from the thermal SiO_2 dielectric. There are two reasons why the turn on voltage is close to 0 V; either there are very few shallow n-type dopant states or a significant density of shallow dopant states are present but are compensated by deep acceptors.

Dopant self-compensation has been invoked as a general explanation of the doping properties of oxides and other wide band gap semiconductors,[31,32] and the mechanism is summarized as follows. The formation energy F_A of an acceptor decreases as the Fermi energy is raised, because the formation of the acceptor moves an electron from the Fermi energy E_F into the acceptor energy level E_A, which is near the valence band. Hence, when the Fermi energy is above the acceptor level and the acceptor is negatively charged, the formation energy is $F_A = F_{A0} - (E_F - E_A)$, where F_{A0} is the formation energy of the neutral acceptor. The energy gain, which could be several eV in a wide band gap semiconductor, reduces the effective formation energy of the acceptor and hence tends to increase the acceptor concentration. The same argument applies to the donor with formation energy F_D and energy level E_D, where a low Fermi energy reduces its formation energy. The dependence on Fermi energy tends to lead to a balance in the donor and acceptor densities, which is shown as follows. The reaction for the formation of a donor and acceptor is

$$\text{bulk} \rightarrow \text{donor} + \text{acceptor} \tag{1}$$

From the law of mass action, the defect densities are given by

$$\begin{aligned} N_D N_A &= N_0^2 \exp[-(F_D + F_A)/kT] \\ &= N_0^2 \exp[-(F_{D0} + F_{A0} - (E_D - E_A)/kT] \end{aligned} \tag{2}$$

where N_0 is the density of atomic sites. For charge neutrality, the densities of donors and acceptors are approximately equal, so that

$$N_D \approx N_A \approx N_0 \exp[-(F_{D0} + F_{A0} - (E_D - E_A)/2kT] \tag{3}$$

The essential point of the self-compensation mechanism is that the defect formation process and the Fermi energy interact so there is a tendency to balance the equilibrium density of donors and acceptors.

Defect formation in a perfect crystal generally occurs in pairs (i.e., a vacancy-interstitial pair), but this is not the case for the sol−gel process or for a nonstoichiometric compound. After the sol−gel material is deposited, a large quantity of the nitrates, acetates, and hydrates are removed to the atmosphere by the high temperature anneal to form the dense film. During the annealing process, oxygen vacancies, interstitials, hydrogen

donors, and possibly several other types of defects and dopants are formed. While the process is chemically very complex, broken bonds and interstitials have many opportunities to diffuse and react during the densification process, so that it is reasonable to consider the defect states as having independent formation energies, rather than being considered as pairs. Those states with particularly low formation energy will be preferentially removed by internal reactions, or diffusion to the surface followed by elimination to the ambient or surface reconstruction. As the material is annealed, defect states will have higher formation energy until some metastable configuration is reached.

This self-compensation mechanism leads us to propose the following model for the properties of solution-based TFTs. Figure 10a illustrates the electronic structure of the oxide semiconductor with a shallow donor and a compensating deep acceptor. As shown by eqs 1−3, it is energetically favorable to form roughly equal concentrations of donors and acceptors. We suppose that the formation energy of these states is relatively low in highly disordered oxygen-rich material where it is easy to form the defects, and increases as the material becomes more ordered and dense by annealing, as illustrated in Figure 10b. Theoretical calculations indeed show that the formation energy of different species depends strongly on whether the material is oxygen-rich or oxygen-poor.[33] Hence, depending on the starting material and the annealing conditions, the density of donors and acceptors decreases until no further densification occurs during the high temperature anneal. As a specific example, an equilibrium concentration of 10^{18} cm^{-3} donors and acceptors by a 400 °C anneal implies that the exponent in eq 3 is about 1.4 eV. Assuming the donor and acceptor levels are 2 eV apart, then $E_{D0} + E_{A0} = 3.4$ eV. This value is consistent with the range of calculated formation energies in oxides.[33,34]

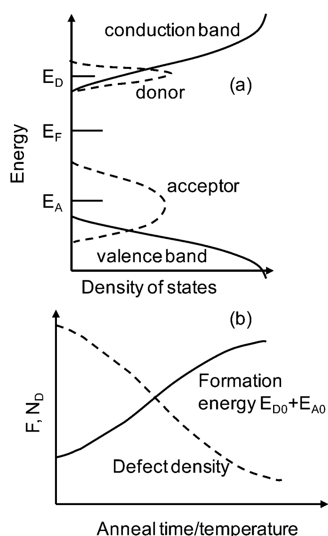


Figure 10. (a) Schematic density of states distribution for the sol−gel oxide semiconductor showing proposed shallow donor and deep acceptor states. (b) Illustration of the increase in defect formation energy F and corresponding reduction in defect density N_D as the sol−gel oxide film is annealed and densifies.

We therefore propose that the difference between low mobility and high mobility material arises from a difference in the final density of donor and acceptor states. Those materials with a high density of these charged states will have larger potential fluctuations than those with a smaller density of states and hence a lower mobility, based on the percolation mechanism. The observed metal composition dependence of the mobility is perhaps related to a variation in the formation energy of one or both of the donor and acceptor states with stoichiometry.

Self-compensation also provides an explanation for the role of the low temperature anneal that shifts the TFT onset voltage toward $V = 0$. The effect arises from the asymmetrical density of states with the shallow donor states lying close to the conduction band but the acceptors further from the valence band. Although the deep Fermi energy position arising from self-compensation ensures that the donor and acceptor states are almost completely ionized and charged, there will also be a significant density of electrons n_E in the conduction band because of its much larger density of states and the high temperature of the anneal, so that

$$n_E = N_C \exp[-(E_C - E_F)/kT] \quad (4)$$

where N_C is the effective density of states at the conduction band edge E_C. Charge neutrality requires that $N_A - N_D = n_E$, so that the self-compensation mechanism actually results in more donors than acceptors. After the device is cooled to room temperature, the excess donors ensure that the oxide is n-type, and hence, the TFTs have a large negative V_{ON}. By performing a final anneal at a low temperature, there is a much smaller density of conduction band electrons, according to eq 4. Hence, the high temperature anneal provides the densification of the structure and the low temperature anneal provides a final adjustment to the self-compensation level. For example, with $N_C = 10^{21}$ cm^{-3} and $E_C - E_F = 0.5$ eV, then n_E is 1.5×10^{17} cm^{-3} at 400 °C but 100× smaller at 180 °C, illustrating that a large turn-on voltage after the 400 °C anneal is greatly reduced after the states equilibrate at 180 °C. The low temperature anneal needs to be done at the lowest temperature that is consistent with the thermal energy needed to allow the structural change needed to modify the states in a reasonable anneal time. The equilibration time is discussed further below.

This proposed self-compensation model does not determine the atomic nature of the donor and acceptor states. The theoretical studies of defects in the oxides suggest that the donor is hydrogen, possibly in the form of an OH bond, and the acceptor may be the oxygen interstitial or metal vacancy.[33,34] The sol−gel process proceeds from metals with an OH termination, and so a residual density of OH bonds seems highly likely. The oxygen vacancy may be present but does not play an obvious role in the self-compensation of the donors and acceptors because it is a deep donor and therefore presumably neutral. The high temperature anneal environment (humid air) is obviously important, but its role in the defect reactions is not clearly understood. The nitrate, acetate, and hydrate components of the sol−gel material are presumably released to the ambient during the high temperature anneal, and the oxygen and water vapor in the ambient may directly interact with the densifying oxide film. Changing the density of donors and acceptors requires a reservoir of states for the exchange. There is plenty of oxygen in the film, but the hydrogen perhaps exchanges with the ambient. The annealing chemistry is evidently complex, and the model we propose is a simplification. It is also unclear to what extent this model relates to oxide films deposited by sputtering. The sputtered film is formed by depositing material with a specific composition, rather than eliminating excess material as for

the sol−gel solution process. However, the high mobility sol−gel oxide TFTs do seem to have similar properties as the sputtered films.

While this model accounts for the mobility in terms of defect processes that are intrinsic to the sol−gel oxide film, there is clearly an additional effect arising from the TFT processing. After the high temperature anneal, processing such as the back channel etch evidently introduces structural damage of some form that is not removed by a subsequent low temperature anneal.

4.2. Bias Stress Effects. The positive gate voltage bias stress effect corresponds to the creation of some form of trapped electrons, which reside in the traps for a long time. There is slow recovery at room temperature and faster recovery at 150−200 °C. The measurements show that the magnitude of the positive stress is closely correlated with the mobility such that TFTs with low mobility exhibit a very strong stress effect, while the highest mobility TFTs are stable. Hence, electron trapping is much more probable and rapid in the low mobility material. A possible model for the positive bias stress is charge trapping of electrons at or in the gate dielectric,[35] but this seems unlikely since the same dielectric exhibits both large and small stress effects. An alternative model is the formation of a negative correlation energy trap state, proposed to be the oxygen vacancy.[36] The idea is that when the state traps two electrons, its configuration changes to a more stable form and there is an energy barrier to the release of the electrons. The energy barrier explains the stability of the stress effect which requires thermal annealing or a long time at room temperature to recover.

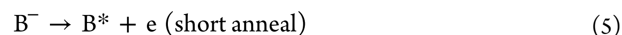
The discussion of donor and acceptor self-compensation suggests an alternative model. Under positive gate bias, electrons accumulate in the channel and the Fermi energy moves to the conduction band. As discussed above, the acceptor formation energy is related to the Fermi energy by $F_A = F_{A0} - (E_F - E_A)$. Hence, the formation energy of the compensating acceptors decreases as the Fermi energy moves up and it is therefore energetically favorable to form more acceptors when the gate bias is positive. The acceptors form slowly due to their large formation energy and remove electrons from the channel, accounting for the slow time dependence of the stress effect. The rate of formation of the compensating acceptors is $\omega_0 \exp[-(F_A/kT)]$, where the prefactor ω_0 is typically $\sim 10^{13}$ s^{-1}. The formation of 10^{17} cm^{-3} acceptors in 10 000 s at room temperature requires a net formation energy of about 1 eV and corresponds to a neutral acceptor formation energy $F_{A0} \sim 3-4$ eV reduced by the electronic energy $E_F - E_A \sim 2-3$ eV. The acceptors are relatively stable at room temperature and so do not recover immediately when the gate bias is removed and the Fermi energy is lower. Instead, the same low temperature (150−200 °C) annealing condition that equilibrates the material after formation restores the self-compensation concentration of donors and acceptors in a short time. This model explains the increased stress effect in the low mobility material because we associate the low mobility with high concentration of donors and acceptors, arising because the formation energy is reduced by the disorder. The low mobility materials should therefore form acceptors by the bias stress effect faster than the high mobility materials which have few donor and acceptor states on account of a higher formation energy. Hence, the observed correlation between bias stress and mobility is accounted for. The model predicts that the positive gate bias stress effect should increase in rate with temperature because the rate of defect formation should be thermally activated.

The NBIS effect is also correlated with the mobility and therefore suggests a similar explanation. In principle, a negative gate bias is expected to move the Fermi energy down which therefore tends to create more donors and hence lead to a negative shift of the TFT characteristics. However, the Fermi energy will not move if the TFT contacts prevent holes from being introduced into the channel. The role of the illumination may therefore be to create holes that participate directly in the defect creation process. The illumination creates hole and electron quasi-Fermi energies (qFE), and the situation is more complex with some different possibilities. For example, instead of creating more shallow donors, the hole qFE changes the occupancy of the acceptors and could reduce their density which would have the same effect as an increase in donors.

The low mobility TFTs have an NBIS behavior characterized by a large negative shift of V_{ON} after a short anneal, as illustrated in Figure 9. After the annealing, V_{ON} is roughly the same for the contacted TFT devices or the noncontacted devices, even though the noncontacted devices have little shift immediately after the light exposure. The observed effects can be explained by supposing that illumination creates both positive and negative charged states

$$\text{light} \rightarrow A^+ + B^- \tag{4}$$

For the TFTs with a gate field, the negative gate bias separates the electrons and holes such that the A^+ states are formed near the dielectric and the B^- states are further into the semiconductor. The separation of the charge creates a dipole field near the TFT interface and hence a threshold shift. For negative illumination stress without a gate field, the same two states are formed but are not separated by the field and so there is little or no threshold shift. The subsequent short anneal either eliminates the B^- states or changes them to neutral states or shallow donors B^*.



$$B^- \rightarrow B^* + e \text{ (short anneal)} \tag{5}$$

As a result, only the A^+ charged states remain and give a large threshold shift of similar magnitude in both contacted and noncontacted devices. Further annealing at 150−200 °C removes the A^+ states, and the threshold shift recovers to its initial value. We do not know the origin of these two types of states, but possible candidates are the oxygen vacancy (+) and oxygen interstitial (−), and states associated with nitrogen or carbon residuals, or hydrogen are also possible.

5. SUMMARY

Oxide semiconductor TFTs in the InGaZn family, processed from solution by the sol−gel method result in TFTs with a wide range of mobility. Devices using the Zn nitrate precursor give better results than the Zn acetate precursor. Mobility values of 20−30 cm^2/(V s) are found for the optimized composition for IGZO and IZO. High mobility is found for devices using shadow mask deposition of the source drain contacts or using an etch stop structure, while liftoff gives slightly lower mobility and a back channel etch process substantially lower mobility. The difference is presumed to relate to etching damage of the channel.

The turn-on voltage of the TFTs is determined in part by a low temperature anneal at the end of the process. In addition, both the positive voltage bias stress and negative bias

illumination stress correlate with device mobility, such that higher mobility devices are more stable with regard to stress. We propose that the mobility, stress, and annealing properties can be explained by a common model involving the thermal generation of self-compensating donor and acceptor states, taking into account the position of the Fermi energy. The model suggests that the process of densification of the sol−gel oxide material by a high temperature anneal increases the defect formation energies and steadily reduces the defect density. A subsequent low temperature anneal adjusts the self-compensation level to approximately equalize the donor and acceptor concentrations and give TFTs with low turn-on voltage.

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This research was financially supported by the Samsung Fine Chemicals Co., Ltd. (RD120067).

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